ABSTRACT OF THE DISCLOSURE

The present invention provides a circuit of processing integer data, especially for graphic applications having a multiplier unit which includes a pipeline in which the word length is adjustable for multiplying integer data s words of 8 bits or multiples thereof an arithmetic logic unit (ALU) for performing arithmetic operations on integer data words, the word length of which is adjustable in 8 bits or multiples thereof; a register unit provided with at least two registers for storage of integer data words having multiples of 8 bits on which the operation and/or pipeline multiplication has to be performed; and a bus structure having a number of separate buses which effects the transport of integer data words from and to the multiplier unit, the arithmetic logic unit and the register unit.